

1 1. A method comprising:

2 defining a multilevel cache including a core

3 having relatively faster components and a region including

4 relatively slower components; and

5 managing the core from said region.

1 2. The method of claim 1 including managing the core

2 from a level 2 cache.

1 3. The method of claim 1 including using a virtual

2 address to index the core to avoid the need for an address

3 translation mechanism.

1 4. The method of claim 1 including placing functions

2 relating to tags and valid bits as well as the data itself

3 in the core.

1 5. The method of claim 1 including using a write-

2 through core cache.

1 6. The method of claim 1 including implementing a

2 line replacement policy in said region.

1 7. The method of claim 1 including performing

2 virtual-to-physical translation in said region.

1 8. The method of claim 1 including handling a core
2 cache miss by passing the details of the access to said
3 region.

1 9. The method of claim 8 including enabling said
2 region to use a memory translation mechanism to determine
3 the physical address and attributes of the access.

1 10. The method of claim 9 including checking to see
2 if the requested data is in a storage associated with said
3 region.

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2 11. An article comprising a medium storing
3 instructions that enable a processor-based system to:
4 define a multilevel cache including a core having
5 relatively faster components and a region including
6 relatively slower components; and
7 manage the core from said region.

1 12. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 manage the core from a level 2 cache.

1 13. The article of claim 11 further storing
2 instructions that enable the processor-based system to use
3 a virtual address to index the core to avoid the need for
4 an address translation mechanism.

1 14. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 access functions relating to tags and valid bits as well as
4 the data itself in the core.

1 15. The article of claim 11 further storing
2 instructions that enable the processor-based system to use
3 a write-through core cache.

1 16. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 implement a line replacement policy in said region.

1 17. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 perform virtual-to-physical translation in said region.

1 18. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 handle a core cache miss by passing the details of the
4 access to said region.

1 19. The article of claim 18 further storing
2 instructions that enable the processor-based system to
3 enable said region to use a memory translation mechanism to
4 determine the physical address and attributes of the
5 access.

1 20. The article of claim 19 further storing
2 instructions that enable the processor-based system to
3 check to see if the requested data is in a storage
4 associated with said region.

1 21. A system comprising:
2 a processor;
3 a multilevel cache including a core having
4 relatively faster components and a region including
5 relatively slower components; and
6 a storage coupled to said processor storing
7 instructions that enable the processor to manage the core
8 from said region.

1 22. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to manage the
3 core from a level 2 cache.

1 23. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to use a
3 virtual address to index the core to avoid the need for an
4 address translation mechanism.

1 24. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to place
3 functions relating to tags and valid bits as well as the
4 data itself in the core.

1 25. The system of claim 21 wherein said core cache is
2 a write-through cache.

1 26. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to implement
3 a line replacement policy in said region.

1 27. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to perform
3 virtual-to-physical translation in said region.

1 28. The system of claim 21 wherein said storage
2 stores instructions that enable the processor to handle a
3 core cache miss by passing the details of the access to
4 said region.

1 29. The system of claim 28 wherein said storage
2 stores instructions that enable the processor to enable
3 said region to use a memory translation mechanism to
4 determine the physical address and attributes of the
5 access.

1 30. The system of claim 29 wherein said storage
2 stores instructions that enable the processor to check to
3 see if the requested data is in a storage associated with
4 said region.